Amendments to the Claims

The listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A method for checking the Cyclic Redundancy Cycle (CRC) of DATA, such DATA comprising a series of data words terminating in a CRC portion, such method comprising:

checking the CRC of the data words while delaying the DATA from passing to an output, each data word in the series being associated with a clock pulse, such delay comprising a plurality of clock pulses;

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corrupting the delayed DATA if such checking determines a CRC error, such corruption of the DATA being performed prior to the data words ~~pass~~ passes to said output; and

checking the output to determine whether there has been a corruption of the delayed DATA..

2. (currently amended) ~~The method recited in claim 1~~ A method for checking the Cyclic Redundancy Cycle (CRC) of DATA, such DATA comprising a series of data words terminating in a CRC portion, such method comprising:

checking the CRC of the data words while delaying the DATA from passing to an output, each data word in the series being associated with a clock pulse, such delay comprising a plurality of clock pulses;

corrupting the delayed DATA if such checking determines a CRC error, such corruption of the DATA being performed prior to the data words pass to said output;

checking the output to determine whether there has been a corruption of the delayed

DATA; and

wherein the corrupting comprising corrupting a parity ~~byte~~ bit of one such data words.

3. (currently amended) A system, comprising;

a source of DATA, such DATA comprising a series of bytes each byte having a parity bit, such series of bytes terminating in a Cyclic Redundancy Cycle (CRC) portion associated with the series of bytes of the DATA;

a source of a the CRC portion;

a CRC checker fed by the series of bytes of the DATA and the source of the CRC portion, for determining a CRC from the seines series of bytes and for comparing such determined CRC with the CRC fed by the CRC source;

a delay fed by the series of bytes and the parity bits thereof;

a selector having a first input thereof fed by the parity bits and a second input thereof fed by the complement of such parity bits, such selector coupling the first input thereof to an output of such selector when the determined CRC is the same as the CRC fed by the CRC source and for coupling the second input thereof to the output when the determined CRC is different from the CRC fed by the CRC source, the output of the selector providing an appended parity bit for the data bytes after such data bytes pass through the delay.

4. (currently amended) A system, comprising;

a source of DATA, such DATA comprising a series of data words, each data word having a parity bit, each data word in the series being associated with a clock pulse, such series of data words terminating in a Cyclic Redundancy Cycle (CRC) portion associated with the series of bytes of the DATA, such CRC portion comprising a predetermined number of CRC words, each one of such CRC words being associated with one of the clock pulses ;

a source of a the CRC portion;

a CRC checker fed by the series of data words and the source of the CRC portion, for

determining a CRC from the ~~seines~~ series of data words and for comparing such determined CRC with the CRC fed by the CRC source;

a delay fed by the series of DATA, such delay delaying the DATA by at least the number of CRC words;

a selector having a first input thereof fed by the parity bits and a second input thereof fed by the complement of such parity bits, such selector coupling the first input thereof to an output of such selector when the determined CRC is the same as the CRC fed by the CRC source and for coupling the second input thereof to the output when the determined CRC is different from the CRC fed by the CRC source, the output of the selector providing an appended parity bit for the data words after such DATA has passed through the delay.

5. (original)The system recited in claim 4 including a second selector, such second selector having a first input fed the DATA and a second input fed by the output of the first-mentioned selector, such second selector coupling either the first input thereof or the second input thereof to an output of the second selector selectively in accordance with a control signal fed to such second selector.